REMARKS

Claims 1-26 are pending in the present application.

Claims 1-26 stand rejected under 35 U.S.C. 102(e) as being anticipated by Gulick et al. (U.S. Patent Number 6,532,019) (hereinafter 'Gulick'). The Applicant respectfully traverses this rejection.

The applicant discloses at page 13, lines 4-12

> "I/O node 100 includes a transceiver unit 110 which is coupled to a link of NC packet interface 50B and to an internal packet bus interface 130 via an internal packet interface link 115. I/O node 100 also includes an I/O hub 120 which is also coupled to internal packet bus interface 130 via an internal packet interface link 125. I/O hub 120 is coupled to peripheral bus 36 and to LPC bus 37. I/O node 100 further includes a graphics bus interface 150 which is coupled to a graphics engine 160 through graphics bus 35. Graphics bus interface 150 is coupled to receive transactions from transceiver unit 110 through internal packet bus interface 130 and internal packet interface link 155. Graphics engine 160 may be connected to a display such as display 38 of FIG. 1." (Emphasis added)

The Applicant also discloses at page 14 line 6-17

> "In a typical computer system, a processor may send graphics commands to an external graphics adapter. In the illustrated embodiment, graphics adapter 35A may include a graphics processor and circuitry (not shown) for generating or rendering digital images and converting the images into signals suitable for use by a display. Graphics adapter 35A may also transmit the digital images for storage in a system memory. Graphics bus interface 150 may be used to translate transactions between the I/O packet interface protocol and a graphics bus protocol such as the AGP protocol, for example. As mentioned above, graphics bus interface 150 may translate bus cycles received from graphics bus 35 into packets for transmission on internal packet interface link 115. In addition, graphics bus interface 150 may translate graphics packets into bus cycles suitable for transmission upon graphics bus 35. ..." (Emphasis added)

The Applicant further discloses at page 15 line 5-17

> "As an alternative to using an external graphics adapter, a **processor may send graphics commands to integrated graphics engine 260 via internal packet interface link 266**. **Graphics engine 260 may include a**

graphics processor and circuitry (not shown) for generating or rendering digital images and converting the images into signals suitable for use by a display. It is contemplated that the graphics signals may be in either an analog or digital format for driving a display such as an RGB monitor or an LCD display. Graphics engine 260 may also include a packet interface circuit (not shown) for translating packets containing digital image information and commands which have been sent via internal packet interface link 266 into signals suitable for use by graphics engine 260. Further the packet interface circuit may translate graphics commands and data into packets for transmission upon internal packet interface link 266." (Emphasis added)

Accordingly, Applicant's claim 1 recites

"an input/output node for a computer system, said input/output node comprising:

a transceiver unit implemented on an integrated circuit chip, wherein said transceiver unit is configured to receive and transmit packets on a point-to-point link of a packet interface;

a graphics engine implemented on said integrated circuit chip, wherein said graphics engine is coupled to receive **graphics packets received by said transceiver unit** and **is configured to render digital image information** in response to receiving said graphics packets; and

an I/O hub implemented on said integrated circuit chip, wherein said I/O hub is coupled to receive I/O packets corresponding to packets received by said transceiver unit and is configured to initiate bus cycles corresponding to said I/O packets upon a peripheral bus." (Emphasis added)

The Examiner asserts that Gulick teaches an I/O node for computer system comprising "a graphics engine implemented on the integrated circuit chip when the graphics engine is coupled to receive graphics packets received by the transceiver unit and is configured to render digital information in response to receiving the graphics packets [see column 3, lines 34-58]."

The Applicant respectfully disagrees with the Examiner's assertion. Specifically, a Gulick teaches at column 3 ,lines 34-58

"In an exemplary embodiment, **processor module 201 provides** the major processing function in the computer system and includes memory

controller 202, one or more central processing units (CPUs) 204, and **graphics controller 206**. Processor module 201 may include one or more integrated circuits. For example, processor module 201 may be a daughter card populated by a number of separate integrated circuits and plugs into a motherboard on which is mounted interface module 203. Alternatively, processor module 201 may be a single integrated circuit. System memory (not shown) is coupled to the memory controller 202. Interface module 203 in the exemplary embodiment shown in FIG. 2 is an **interface module that functions as an I/O hub** by providing an interface between various input/output devices such as hard drives, scanners, printers, network connections, modems etc., and the processor module. **The exemplary I/O module 203 includes** ISA interface 230 (providing an interface to the industry standard architecture (ISA) bus), IEEE 1394 interface 232, Peripheral Component Interconnect bridge (PCI) 234, Intelligent Drive Electronics (IDE) controller 236, and **RAMDAC 238. In the exemplary embodiment interface module 203 is a single integrated circuit.** Other types of buses and input/output devices may also be present on interface module 203 in place of or in addition to those described." (Emphasis added)

Gulick also teaches at column 7, lines 47-63

"The computer system integrates CPU 204, graphics controller 206 and memory controller 202 onto processor module 201. **Processor module 201 connects to interface module 203 via link 209**. Note that link 209 may operate in accordance with one of the embodiments described herein or be another high speed link, e.g., a fiber optic link, that is capable of meeting throughput and latency requirements where high-bandwidth asynchronous traffic must be mixed with isochronous traffic. Interface module 203 provides an I/O hub for the computer system and may also provide other functions not illustrated, such as power management functions.
The key aspect of interface module 203 relevant to the present invention is the presence of RAMDAC 238. RAMDAC 238 converts the digital screen image from the frame buffer into analog data, which is provided to display 252." (Emphasis added)

From the foregoing, Gulick teaches a processor node that includes a graphics engine (graphics controller 206) and an interface module that includes a RAMDAC 238. The Applicant notes that a RAMDAC **is not** a graphics engine. As taught by Gulick, a RAMDAC merely converts a digital screen image (that has already been rendered) into signals suitable for display. Accordingly, Gulick does not to teach or disclose "a graphics engine implemented on said integrated circuit chip, wherein said graphics engine is

coupled to receive graphics packets received by said transceiver unit..." as recited in Applicant's claim 1. In addition, Gulick does not teach or disclose a graphics engine and an I/O node both implemented on the same integrated circuit chip wherein the I/O node is "coupled to receive I/O packets corresponding to packets received by said transceiver unit..." as recited in Applicant's claim 1.

Furthermore, applicant's claim 3 recites "a graphics bus interface implemented on said integrated circuit chip, wherein said graphics bus interface is coupled to receive and to translate said graphics packets into graphics commands suitable for transmission upon a graphics bus." The applicant respectfully submits that the I/O node includes both a graphics bus interface and a graphics engine.

The applicant respectfully submits that claim 1, along with its dependent claims, patentably distinguishes over Gulick for the reasons given above.

Claim 10 recites a computer system that includes features that are similar to the features recited in claim 1. Thus, the Applicant submits that claim 10, along with its dependent claims, patentably distinguishes over Gulick for at least the reasons given above.

Applicant also discloses at page 14 line 21 through page15 line 9

> **"As an alternative to using an external graphics adapter**, a processor may send graphics commands to **integrated graphics engine 160** via graphics bus interface 150. **Graphics engine 160 may include a graphics processor and circuitry (not shown) for generating or rendering digital images and converting the images into signals suitable for use by a display**. It is contemplated that the graphics signals may be in either an analog or digital format for driving a display such as an RGB monitor or an LCD display. Graphics engine 160 may also include a bus interface (not shown) for transmitting and receiving digital image information and commands on graphics bus 35 thereby allowing the transmission of the digital images for storage and subsequent retrieval in a system memory. Graphics engine 160 also includes a control register 165 which may be configured to selectively enable or disable graphics engine 160. In addition, it is contemplated that control register 165 may be

configured to select other graphics related functions such as display resolution and timing, for example. Since in typical computer systems only one graphics processor may be in use at a given time, graphics engine 160 may be disabled using control register 165 while an external graphics adapter (e.g. graphics adapter 35A) is used. Alternatively, graphics engine 160 may be enabled when there is no external graphics adapter being used." (Emphasis added)

Accordingly, claim 19 recites an input/output node for a computer system comprising, in pertinent part,

"a graphics bus interface implemented on said integrated circuit chip, wherein said graphics bus interface is coupled to receive packets including graphics commands and to translate said packets into graphics commands suitable for transmission upon a graphics bus.

a graphics engine implemented on said integrated circuit chip and coupled to said graphics bus, wherein said graphics engine is coupled to receive said graphics commands via said graphics bus and is configured to render digital image information in response to receiving said graphics commands; and

an I/O hub implemented on said integrated circuit chip, wherein said I/O hub is coupled to receive I/O packets corresponding to packets received by said transceiver unit and is configured to initiate bus cycles corresponding to said I/O packets upon a peripheral bus." (Emphasis added)

Gulick does not teach or disclose "a graphics bus interface implemented on said integrated circuit chip, wherein said graphics bus interface is coupled to receive packets including graphics commands and to translate said packets into graphics commands suitable for transmission upon a graphics bus," "a graphics engine implemented on said integrated circuit chip and coupled to said graphics bus, wherein said graphics engine is coupled to receive said graphics commands via said graphics bus...," and "an I/O hub implemented on said integrated circuit chip," as recited in Applicant's claim 19.

Thus, Applicant submits that claim 19, along with its dependent claims, patentably distinguishes over Gulick for at least the reasons given above.

CONCLUSION

Applicant submits the application is in condition for allowance, and an early notice to that effect is requested.

If any fees are due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C. Deposit Account No. 501505/5500-73600/BNK.

Respectfully submitted,

Stephen J. Curran
Reg. No. 50,664
AGENT FOR APPLICANT(S)

Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C.
P.O. Box 398
Austin, TX 78767-0398
Phone: (512) 853-8800

Date: 7/7/04